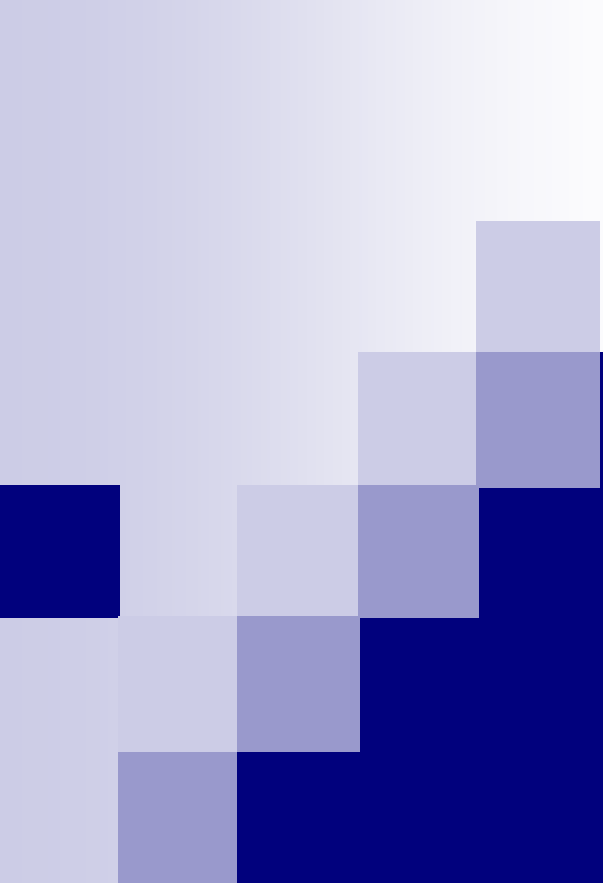




Implementation of 8-bit adder

Rashmi Kumar

Administrative

- This lab requires a report
- Two 15-Sep-03week lab
- Has a Pre-lab – so please be prepared
- You will need the User Guide for the Altera UP2 board – so please print a copy

Objective of the lab

- Design a 8-bit adder which is capable of:
 - Taking two 8-bit numbers from the DIP switches
 - Display the result on the seven segment display
 - Provide a visual feedback when overflow occurs

Equipment

- Altera UP2 Development Board
- Max-plus-II Integrated Design Environment (Software)

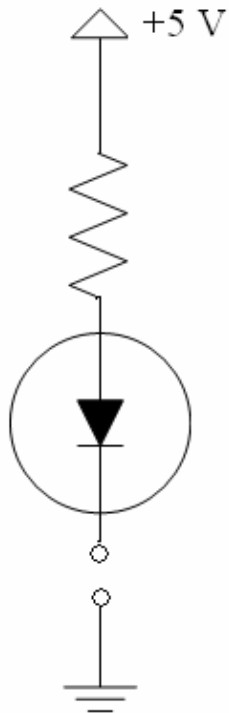
Suggested Design Flow

- Write a Verilog code for the 8-bit adder and the hex to seven segment display
 - Several ways to do this
 1. Make two functional units – one for the adder, another for the hex-to-seven segment display
 2. Make a single unit that incorporates both addition and conversion
- Create a symbol for each block

Design Flow (cont.)

- Integrate your design as a top-level design in the graphical editor
- Functional Simulation – make sure that your design is logically correct!
- Major Consideration:
 - All UP2 peripherals are driven active-low

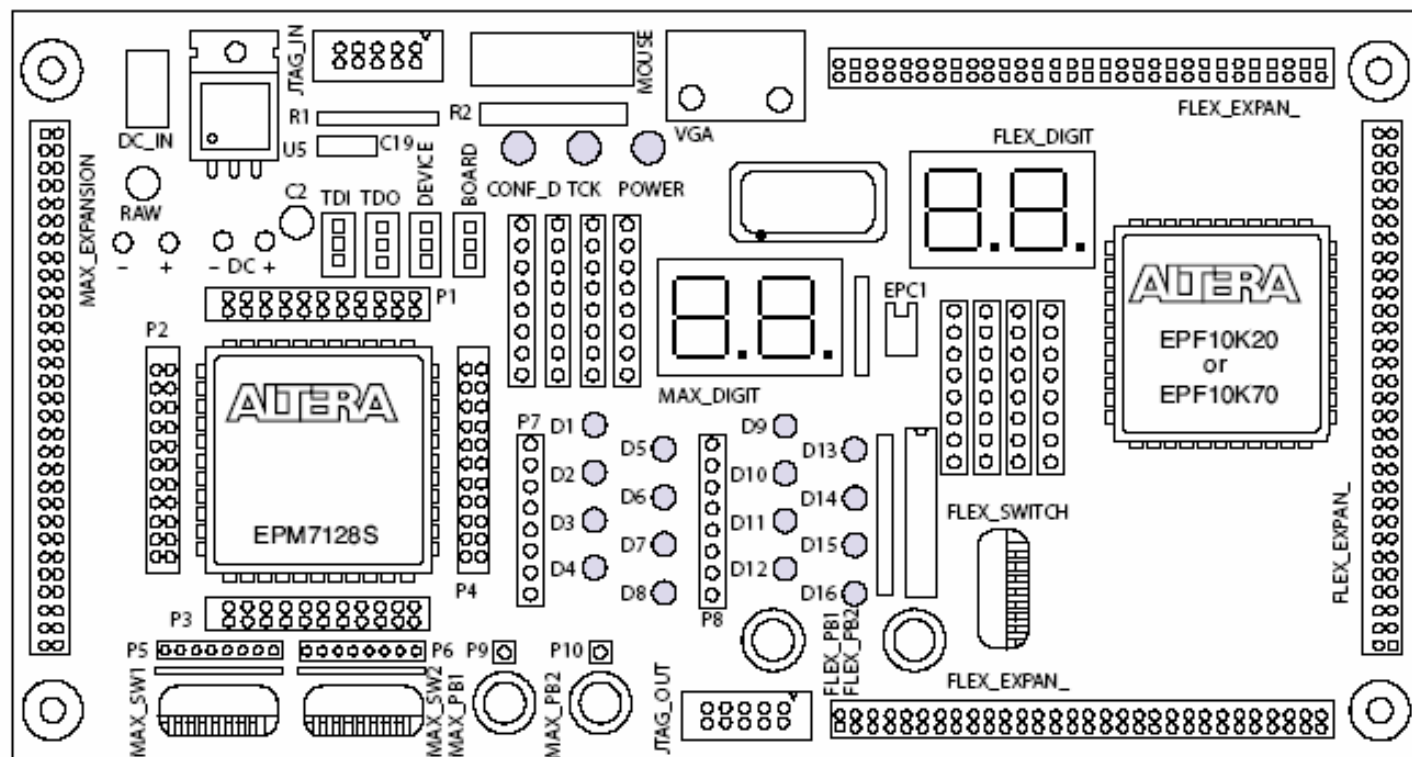
Active-low signaling



- Pull up resistors
- For example – 10-K Ω resistors for dip switches
- 16 LEDs pulled up 330 Ω resistors

The UP2 board

Figure 1. UP Education Board Block Diagram



Things to keep in mind

- Recommended FPGA EPM7128S
- LEDs are hardwired to the MAX chip
- DIP switches are not – so you will need to physically wire them (hook-up wires)
- User manual has a list of pin connections
 - MAX_DIGIT display – seven segment display directly connected to EPM7128S

Things to keep in mind

Figure 4. Display Segment Name

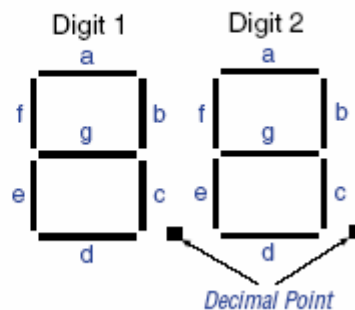


Table 4 lists the pin assignments for each segment.

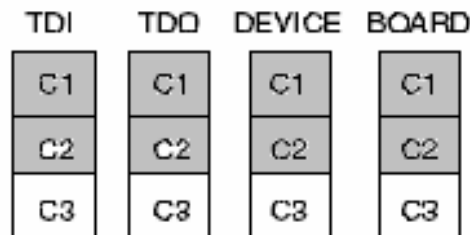
Table 4. MAX_DIGIT Segment I/O Connections		
Display Segment	Pin for Digit 1	Pin for Digit 2
a	58	69
b	60	70
c	61	73
d	63	74
e	64	76
f	65	75
g	67	77
Decimal point	68	79

Ref: University Program Design Laboratory Package User Guide – Altera Corp.

Things to keep in mind

■ Jumper Settings

- ☐ Set the JTAG configuration
- ☐ JTAG chain can be configured to be connected to any device
- ☐ To program only EPM7128S



Position of C1, C2 & C3 Connectors

Downloading to the chip

- Functional Analysis
- Verify your design (waveform editor)
- Device Selection
- Pin Assignments
- Compile the program
- Program the Device – follow the instructions from the User Manual

Test your design!

- If you programmed correctly and transferred the design to the FPGA successfully [Configuration Complete] – you should be able to feed in two 8-bit numbers through the DIP switches, see the sum on the 7 segment display AND see the overflow, if it occurs
(Hint: LED or dp lights up!! or you can be innovative and have an error message displayed on the 7 segment display unit!!)



You are all set for next week's lab!! 😊